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IN THE CLAIMS:

Please amend claims 1, 3-11, 15-16 and 18-20, and add a new claim 21 as follows:

1. (Currently Amended) A semiconductor integrated circuit having at least one self-construction circuit, said self-construction circuit comprising:
storing means ~~that enables~~ for reading data therefrom and writing data thereinto;
comparing means for providing a comparison result ~~that compare write data supplied to the storing means with data read from the storing means~~; and
variable address converting means ~~that~~ for converting an address signal inputted to said self-construction circuit ~~supplied into a write address in the storing means~~ for writing into the storing means input data of a hardware description language statement of a newly designated logical function based on ~~[[a]]~~ the comparison result ~~in~~ by the comparing means,
wherein said comparing means compare input data continuously supplied to said self-construction circuit with the input data written into and then read from the storing means ~~an input signal of a logic circuit having a desired logical function is input as the address signal to the storing means~~, and
wherein the input data is written to the storing means so that ~~the read data~~ read from ~~of the storing means can be obtained as is~~ an expected output signal according to the newly designated logical function with respect to ~~the~~ an input signal of the self-construction logic circuit.
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2. (Original) ^{The} A semiconductor integrated circuit according to claim 1, wherein a plurality of the storing means, a plurality of the comparing means, and a plurality of the variable address converting means are provided on a single semiconductor chip.
3. (Currently Amended) ^{The} A semiconductor integrated circuit according to claim 1, wherein the storing means are include a volatile memory.
4. (Currently Amended) ^{The} A semiconductor integrated circuit according to claim 1, wherein the variable address converting means comprise:

a memory array in which a plurality of memory cells are arranged in a matrix shape;

an address decoder that selects the memory cells in the memory array based on an input address signal;

reading amplifying means that for amplifying a signal read from the memory array; and

operating updating means that for updat[[e]]ing the input address signal based on a control signal.

5. (Currently Amended) ^{THE} A semiconductor integrated circuit according to claim 4, wherein the memory array ~~has the~~ is a volatile memory.
6. (Currently Amended) ^{THE} A semiconductor integrated circuit according to claim 1, 2, 3, 4, or 5, further comprising: data holding means ~~that can~~ for holding ~~the~~ data read from the storing means; a switch matrix ~~that~~ for switch[[es]]ing the input address signal or an output signal of the data holding means and ~~for can~~ supplying the switched signal ~~it~~ to the variable address converting means[[;]] and to the storing means, wherein the storing means ~~that~~ store the control information of each switch in the switch matrix.
7. (Currently Amended) ^{THE} A semiconductor integrated circuit according to claim 6, wherein the data holding means comprise:
- latching means ~~that can~~ for latching first data read from the memory array ~~circuit~~;
- and
- gate means ~~that permit or do not permit~~ for determining whether to latch[[ing of]] the first data ~~to~~ by the latching means based on the first data read from the memory array ~~circuit~~.
8. (Currently Amended) A method for constructing a logic integrated circuit, ~~wherein~~ comprising:
- providing at least one self-construction circuit capable of being converted to operating different logical functions as a building block for the logic integrated circuit;
- assigning a desired logical function to said self-construction circuit by sending an address

signal to the self-construction circuit;

self-decoding design data coded at logical function level of the desired logical function by the self-construction circuit;

self-converting by the self-construction circuit to operate according to the desired logical function; and

self-verifying by the self-construction circuit with the desired logical function the logic integrated circuit having a desired logical function is constructed by decoding design data of a function level described in HDL by control means using the semiconductor integrated circuit according to claim 1, 2, 3, 4, 5, 6, or 7 and assigning to the self construction circuit a signal that decides a logical configuration of a self construction circuit capable of constructing optional logic from the control means.

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9. (Currently Amended) A method for constructing the logic integrated circuit according to claim 8, wherein the control means for decoding the design data are formed on the same an identical semi-conductor chip as the self-construction circuit.
 10. (Currently Amended) A method for constructing the logic integrated circuit according to claim 9, wherein a storage that stores memory for storing the design data of the coded at logical function level ~~are~~ is formed on the same an identical semiconductor chip as the control means and the self-construction circuit.
 11. (Currently Amended) A semiconductor integrated circuit having at least one self-construction circuit, said self-construction circuit comprising:
storing means that hold for storing information obtained from a description in which a newly assigned logical function is represented in a hardware description language and for obtaining the an output of according to the newly assigned logical function with respect to an input signal supplied to an address terminal thereof; and
means for verifying a correlation between the output signal and the input signal that complies complying with the newly assigned logical function an input signal from the output terminal, using the signal supplied to the address terminal as the input signal.
 12. (Original) A semiconductor integrated circuit according to claim 11, wherein the logical

function includes a combinational logical function.

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13. (Original) A semiconductor integrated circuit according to claim 12, wherein the logical function includes a sequential logical function.
 14. (Original) A semiconductor integrated circuit according to claim 11, wherein the storing means are read- and write-enable storing means.
 15. (Currently Amended) A semiconductor integrated circuit according to claim 11, wherein the means for verifying includes converting means ~~that from~~ for converting into the information written to the storing means from the description represented in the hardware description language ~~and the storing means are formed on the same semiconductor chip.~~
 16. (Currently Amended) A semiconductor integrated circuit according to claim 15, wherein the storing means ~~that hold~~ stores the description represented in the hardware description language ~~are formed on the semiconductor chip.~~
 17. (Previously Presented) A semiconductor integrated circuit according to claim 2, wherein the storing means are a volatile memory.
 18. (Currently Amended) A semiconductor integrated circuit according to claim 2, wherein the variable address converting means comprise:
 - a memory array in which a plurality of memory cells are arranged in a matrix shape;
 - an address decoder that selects the memory cells in the memory array based on an input address signal;
 - ~~reading~~ amplifying means that for amplifying a signal read from the memory array; and
 - ~~operating~~ updating means that for updat[[e]]ing the input address signal based on a control signal.

19. (Currently Amended) A semiconductor integrated circuit according to claim 3, wherein the variable address converting means comprise:

a memory array in which a plurality of memory cells are arranged in a matrix shape;

an address decoder that selects the memory cells in the memory array based on an input address signal;

reading amplifying means ~~that~~ for amplifying a signal read from the memory array; and

operating updating means ~~that~~ for updat[[e]]ing the input address signal based on a control signal.

20. (Currently Amended) A semiconductor integrated circuit according to claim 4, wherein the variable address converting means comprise:

a memory array in which a plurality of memory cells are arranged in a matrix shape;

an address decoder that selects the memory cells in the memory array based on an input address signal;

reading amplifying means ~~that~~ for amplifying a signal read from the memory array; and

operating updating means ~~that~~ for updat[[e]]ing the input address signal based on a control signal.

21. (New) ^{THE} A method for constructing the logic integrated circuit according to claim 8, wherein the steps ^{of what} by said self-construction circuit involves:

converting the address signal inputted into a write address;

comparing input data continuously supplied to said self-construction circuit with the input data written into and then read from the self-construction circuit; and

writing into said self-construction circuit input data of the desired designated logical function into the write address based on a result determined in the comparing step.